REMARKS

Claims 1-3 have been amended. New dependent claim 11 has been added. No new matter has been added to the application by virtue of the present amendments. Accordingly, claims 1-11 are pending in the subject application. It is respectfully requested that such pending claims 1-11 be reconsidered and passed to issuance in view of this response.

Information Disclosure Statement

The Examiner indicated that the listing of references in the specification was not proper and requested that the references be submitted by separate paper [MPEP§609A(I)]. The Administrative Assistant to the undersigned called the Examiner on April 15, 2002, to explain that an IDS Form PTO-1449 was filed in the subject patent application on August 1, 2001, which listed and attached the references in question. The Examiner indicated that a search of the file would be accomplished and she would request an addition copy, if required.

Claim Rejections – 35 U.S.C. 112, second paragraph

The Examiner rejected claims 2 and 3 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Regarding claim 2, Applicants have amended claim 2 to more clearly define the subject matter which Applicant regards as the invention.

Regarding claim 3, Applicants have amended claim 3 to delete the term "substantially".

Therefore, Applicants believe the rejections under 35 U.S.C. 112, second paragraph, have been overcome.

Claim Rejections – 35 U.S.C. 102 (b)

The Examiner rejected claim 1 under 35 U.S.C. 102(b) as being anticipated by Sasaki (JP-10070234), and claims 1-8 and 10 as being anticipated by Garbelli et al. (U.S. Patent No. 5,825,628).

Regarding independent claim 1, Applicants have amended claim 1 to recite the limitations of "... an electrically insulating layer between said die and said ground plane ...". Referring to FIG. 1 (paragraph 0061) of the present application, Applicants teach air layer 23

between die 20 and ground plane 22. In FIG. 2 (paragraph 0062), Applicants teach mold 35 (encapsulant) between die 38 and ground plane 40. In FIG. 3 (paragraph 0063), Applicants teach bonding layer 57 and intervening mounting material layer 61 between die 60 and ground plane 65. The switching noise current of the power circuit of the die creates a loop current within the IC package which creates electromagnetic fields. Applicants' invention provides a ground plane which is electrically isolated from the die so that the electromagnetic fields can be confined to within the IC package (FIG. 4, paragraph 0064). Applicants' ground plane provides an electrical path to ground for the electromagnetic fields. In addition, since the ground plane is electrically isolated from the die, signals to and from the die are isolated from noise generated on the ground plane from the electromagnetic fields.

Sasaki neither anticipates nor suggests Applicants' claim 1, as amended. As shown in FIG. 1 of Sasaki, Sasaki teaches IC chip 3 connected directly to die pad 4. Since die pad 4 is made of a conductive material, die pad 4 becomes a part of the loop current path created by the switching noise of IC chip 3. Thus, die pad 4 actually helps to create electromagnetic fields which radiate out of IC package 1 rather than prevent electromagnetic radiation out of IC package 1.

Garbelli et al. neither anticipate nor suggest Applicants' claim 1, as amended. As shown in FIG. 3 of Garbelli et al., Garbelli et al. teach conductive pads 212-218 adjacent chip 110, conductive holes 326, 328 through substrate 310 and connected to conductive pads 212-218, and conductive pads 336, 338 connected to conductive holes 326, 328 and adjacent an outer surface of substrate 310. A loop current created in package 300 of Garbelli et al. would result in electromagnetic fields having multiple electrical paths, such as pad 216-conductive pad 326-conductive pad 336, to radiate out of package 300.

Therefore, Applicants believe the rejections under 35 U.S.C. 102(b) have been overcome.

Claim Rejections – 35 U.S.C. 103 (a)

The Examiner rejected claim 9 under 35 U.S.C. 103(a) as being unpatentable over Garbelli et al. (U.S. Patent No. 5,825,628) in view of Hernandez et al. (U.S. Patent No. 4,734,818).

As discussed above, Garbelli et al. do not teach Applicants limitation of "... an electrically insulating layer between said die and said ground plane ..." in claim 1, as amended. Claim 9 is dependant upon claim 1, as amended. Thus, the combination of Garbelli et al. with Hernandez et al. does not teach or suggest Applicants' claim 9.

For the foregoing reasons, claim 9 is neither taught nor suggested, either individually or in combination, by Garbelli et al. or Hernandez et al. and are believed to be allowable over

Garbelli et al. in view of Hernandez et al. Accordingly, Applicants respectfully request that the rejection of claim 9 over Garbelli et al. in view of Hernandez et al. be reconsidered and withdrawn.

Prior Art Made of Record

The prior art made of record by Examiner and not relied upon, i.e. Bhattacharyya et al., Kabumoto et al., Hundt, Suzuki et al., Khandros et al. and Takeuchi, have been reviewed and do not anticipate or suggest the elements of pending independent claim 1, as amended.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

In light of the foregoing amendment and remarks, all of the claims now presented are believed to be in condition for allowance, and Applicants respectfully request that the outstanding rejections be withdrawn and this application be passed to issue at an early date.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 1-3 have been amended as follows:

1. (Once Amended) A semiconductor integrated circuit device comprising:

a die connected to a ground lead and a power lead;

a ground plane connected to the ground lead;

an electrically insulating layer between said die and said ground plane;

a decoupling capacitor having a first end and a second end, the first end connected to the ground lead and the second end connected to the power lead; and

an encapsulating material for encapsulating the die, the ground plane, the electrically insulating layer and the decoupling capacitor.

2. (Once Amended) The semiconductor integrated circuit device according to Claim 1, wherein said ground plane is adjacent a first plane ~~facing~~ of a printed circuit board for mounting electronic parts ~~and a second plane facing opposite to said printed circuit board for mounting electronic parts in said semiconductor integrated circuit device are defined as a bottom surface and a top surface, respectively, and said ground plane extends along said bottom surface~~.

3. (Once Amended) The semiconductor integrated circuit device according to Claim 2, wherein said ground plane extends in two dimensions ~~substantially throughout said bottom surface~~ beyond the edges of said die.